a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

C1 cancel'd.

(c) a third step of annealing the oxide films at a substrate temperature [of] which is greater than 1100°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1/μm2.

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25. (Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising the steps of:

Amend

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) depositing oxide films in the grooves by an organic silicon based CVD method;

(c) annealing the oxide films at a substrate temperature [of] which is greater than 1100°C but less than or equal to 1350°C so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than $1/\mu m^2$; and

C2

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

26. (Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by an organic silicon based CVD method; and

(c) annealing said oxide films at a substrate temperature [of] which is greater than

1100°C but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of said oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

27. (Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by an organic silicon based CVD method; and

(c) annealing the oxide films at a substrate temperature [of] which is greater than 1100°C but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the ring structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially more than 85% of an overall ring structure and said lower order ring structures are substantially less than 15% of the overall ring structure.

28. (Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films as part of inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by an organic silicon based CVD method;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(e) annealing the oxide films at a substrate temperature [of] which is greater than 1100°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^2$.

29. (Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films as part of inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by an organic silicon based CVD method;

(d) annealing the oxide films at a substrate temperature [of] which is greater than 1100°C but less than or equal to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than $1/\mu m^2$; and

(e) removing upper parts of the oxide films so as to planarize a surface of the resulting structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top